IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Previously Presented): A phase detector comprising:

a first selection circuit configured to select a first clock from a first group of clocks supplied to the first selection circuit and to transmit the first clock;

at least one phase comparator configured to detect a difference in phases between the first clock and a second clock supplied to the phase comparator and to transmit the difference as a scan signal;

a first latch configured to receive the scan signal and to store the scan signal when a third clock is supplied to the first latch; and

a second latch configured to store the scan signal when a reverse phase of the third clock is supplied to the second latch.

Claim 2 (Original): The phase detector of claim 1, further comprising a second selection circuit configured to select the second clock from a second group of clocks and to transmit the second clock to the phase comparator.

Claim 3 and 4 (Canceled).

Claim 5 (Currently Amended): The phase detector of claim 1, further comprising:

an AND gate configured to pass [[a ]] the third clock through when the first clock and the second clock are in-phase; and

a first flip-flop configured to divide the third clock by two and to transmit the divided clock as a fourth clock.

Claim 6 (Currently Amended): The phase detector of claim 2, further comprising:

an AND gate configured to pass [[a ]] the third clock through when the first clock and the second clock are in-phase; and

a first flip-flop configured to divide the third clock by two and to transmit the divided clock as a fourth clock.

Claim 7 (Canceled).

Claim 8 (Previously Presented): The phase detector of claim 5, further comprising: a second flip-flop configured to divide the fourth clock by two and to transmit the divided clock as a fifth clock to the second selection circuit.

Claim 9 (Previously Presented): A clock distribution circuit comprising:

a plurality of domain clock buffers configured to supply clocks to logic elements;

a first selection circuit configured to select a first clock from a first group of the clocks supplied from the domain clock buffers and to transmit the first clock;

at least one phase comparator configured to detect a difference in phases between the first clock and a second clock supplied to the phase comparator and to transmit the difference as a scan signal;

a first latch configured to receive the scan signal and to store the scan signal when a third clock is supplied to the first latch; and

a second latch configured to store the scan signal when a reverse phase of the third clock is supplied to the second latch.

Claim 10 (Original): The clock distribution circuit of claim 9 wherein each of the phase comparators is coupled with the domain clock buffers with the same propagation delay from the domain clock buffers.

Claim 11 (Currently Amended): The clock distribution circuit of claim 9, further comprising a second selection circuit configured to select [[a]] the second clock from a second group of the clocks and to transmit the second clock to the phase comparator.

Claim 12 (Canceled).

Claim 13 (Currently Amended): The clock distribution circuit of claim 9, further comprising:

an AND gate configured to pass [[a ]] the third clock through when the first clock and the second clock are in-phase; and

a first flip-flop configured to divide the third clock by two and to transmit the divided clock as a fourth clock.

Claim 14 (Original): The clock distribution circuit of claim 9, further comprising a deskew circuit configured to calculate a propagation delay of the clock from the domain clock buffer and to adjust a clock skew of the domain clock buffers.

Claim 15 (Previously Presented): A LSI comprising:

a plurality of divided domains in the LSI area;

at least one clock buffer configured to supply clocks to logic elements in the domains;

a first selection circuit configured to select a first clock from a first group of the clocks supplied from the domain clock buffers and to transmit the first clock; at least one phase comparator configured to detect a difference in phases between the first clock and a second clock supplied to the phase comparator and to signal the difference as a scan signal;

a first latch configured to receive the scan signal and to store the scan signal when a third clock is supplied to the first latch; and

a second latch configured to store the scan signal when a reverse phase of the third clock is supplied to the second latch.

Claim 16 (Original): The LSI of claim 15 wherein each of the phase comparators are located at intersections of two boundaries of the domains.

Claim 17 (Currently Amended): The LSI of claim 15, further comprising a second selection circuit configured to select [[a]] the second clock sequentially from a plurality of a second group of the clocks and to transmit the selected clock to the phase comparator.

Claim 18 (Canceled).

Claim 19 (Currently Amended): The LSI of claim 15, further comprising:

an AND gate configured to pass [[a ]] the third clock through when the first clock and the second clock are in-phase; and

a first flip-flop configured to divide the third clock by two and to transmit the divided clock as a fourth clock.

Claim 20 (Original): The LSI of claim 15, further comprising: a deskew circuit configured to calculate a propagation delay of the clock from the domain clock buffer and to adjust a clock skew of the domain clock buffers.